Amendments to the specification:

Please amend the paragraph on page 113, lines 9-20 as follows:

Fig. 23 shows an example of ~~the~~ a latch circuit LAT that constitutes ~~the~~ a shift register circuit ~~mentioned in claim 23~~according to the present invention. In Fig. 23, the p-type transistors M11 and M12, the n-type transistors M13 through M18 and the first and second clock signal input control sections 15 and 16 have the same constructions and functions as those of the p-type transistors M11 and M12, the n-type transistors M13 through M18 and the first and second clock signal input control sections 12 and 13 of Fig. 3. It is to be noted that the concrete circuit constructions of the first and second clock signal input control sections 15 and 16 are as shown in Fig. 19 through Fig. 22.

Please amend the paragraph on page 115, line 22 to page 117, line 3 as follows:

Fig. 25 is a block diagram showing an example of ~~the~~ a shift register circuit ~~mentioned in claim 20~~according to the present invention. In this shift register circuit 21, the output nodes and input nodes of adjacent latch circuits LAT are connected via analog switches ASW. That is, a start signal (pulse signal) st is inputted to the input node of the latch circuit LAT of the first stage via an analog switch ASW1 that is controlled to be turned on and off by an external control signal lr. On the other hand, the output node is connected to the input node of the latch circuit LAT of the second stage via the analog switch ASW1. Next, the input node of the latch circuit LAT of the second stage is connected to the output node of the latch circuit LAT of the third stage via an analog switch ASW2 that is controlled to be turned on and off by an external control signal /lr besides the output node of the latch circuit LAT of the first stage. On the other hand, the output node is connected to the input node of the latch circuit LAT of the first stage via the analog switch ASW2 and connected to the input node of the latch circuit LAT of the third stage via the analog switch ASW1. Next, the input node of the latch circuit LAT of the third stage is connected to the output node of the latch circuit LAT of the fourth stage via the analog switch

ASW2 besides the output node of the latch circuit LAT of the second stage. On the other hand, the output node is connected to the input node of the latch circuit LAT of the fourth stage via the analog switch ASW1 besides the input node of the latch circuit LAT of the second stage. Then, the start signal st is inputted via the analog switch ASW2 to the input node of the latch circuit LAT of the fourth stage, or the final stage besides the output signal from the latch circuit LAT of the third stage.

Please amend the paragraph on page 119, lines 4-12 as follows:

Fig. 27 is an example of ~~the~~ a shift register circuit ~~mentioned in claim 21~~according to the present invention, showing a modification example of the shift register circuit described with reference to Fig. 25. In this shift register circuit, buffer circuits BUF are additionally provided between the outputs of the latch circuits LAT and the analog switches ASW1 and ASW2 that serve as the first and second transfer gates toward the latch circuits of the preceding stages and the succeeding stages.